
Upgrading CO561AD-x Designs to CO661AL-x

Introduction

The CO661AL-x is a new and advanced iChip family of Internet Controllers designed to be backward compatible with the CO561AD-x iChip family. Most existing designs incorporating the CO561AD devices will accept the CO661AL devices with little or no change. This document describes the differences between the device families and provides design guidelines to ensure easy replacement of the CO561AD with the more advanced CO661AL. Where applicable, some existing CO561AD design changes may be required. This document is intended to point out these potential change requirements.

CO661AL-x Features and Functionality

The CO661AL-x family is designed for high-bandwidth applications. In serial host interface mode, it will support 230 kbps bandwidth. In addition, CO661AL-L and CO661AL-D will include a Parallel host interface with support for 500 Kbytes/Sec burst and up to 400 Kbytes/Sec sustained bandwidth¹. Because CO661AL is based on an ARM7TDMI processor, it uses code more efficiently than the CO561AD's 186 core, which limits the ability to add more functionality to the CO561AD. Thus, many of iChip's new features, such as support for 10/100BaseT, 802.11b and security, will only be available on the CO661AL. The new CO661AL-x family also features power save modes that are not available on the CO561AD. The CO661AL-x family will also be available in an extended temperature range version, which will not be available for the CO561AD-x family.

Power

Unlike the CO561AD-x iChip family, which is offered in two operating voltages: +5VDC or +3.3VDC, the CO661AL-x is offered only in +3.3VDC. Existing CO561AD-x +5VDC designs will require a change of voltage regulator and possibly several discrete components, if replaced by a CO661AL-x. In addition, CO661AL-x power dissipation is significantly lower than that of the CO561AD-x family. While the CO561AD-x +3.3VDC devices consume 70mA, the CO661AL-x devices consume only 30mA during peak performance. Moreover, the CO661AL-x devices have a power save mode, which drops the power consumption to 10mA when the device is idle. CO661AL-x will also have a dedicated signal (PWSG) to achieve sleep mode (via an external circuit) that will reduce power consumption below 1 mA.

Core Processor

The CO661AL-x devices are based on an ARM7TDMI core, whereas the CO561AD-x devices incorporate an x186 core.

Note: 1-- Maximum sustained bandwidth measured by streaming data over a UDP socket.

Parallel Host Interface

The CO661AL-x family is designed to support an 8-bit parallel host interface. This will provide an alternative interface for processors that do not have an available serial port, as well as support high bandwidth in LAN applications (up to a peak of 400 Kbytes/Sec sustained). The CO661AL-x family will contain parallel mode drivers starting in major firmware version 801, expected early 2003. The CO661AL-x devices reset to parallel mode when pin 55 (-SER/PAR) is pulled high. When in parallel mode, several CO661AL pin definitions are different. Please refer to the CO661AL-x data sheets (Connect One Documents 11-3400-xx, 11-3600-xx & 11-3800-xx) for additional information. Backwards compatibility to CO561AD-x devices is ensured, as CO561AD-x pin 55 is a GND pin and should always boot in a LOW state.

Reset Profile

The CO561AD-x and CO661AL-x require a slightly different reset signal profile to ensure a clean reset. Minimum V_{ih} in CO561AD-x is 2.4V compared to 2.0V on CO661AL-X. If the reset circuit is an RC network, this must be taken into consideration.

The first AT+i command may be issued to the CO561AD-x at least 4 sec after reset and to the CO661AL-x at least 1 sec after reset.

The following timing charts depict the required reset profile for each device family when using an RC network:

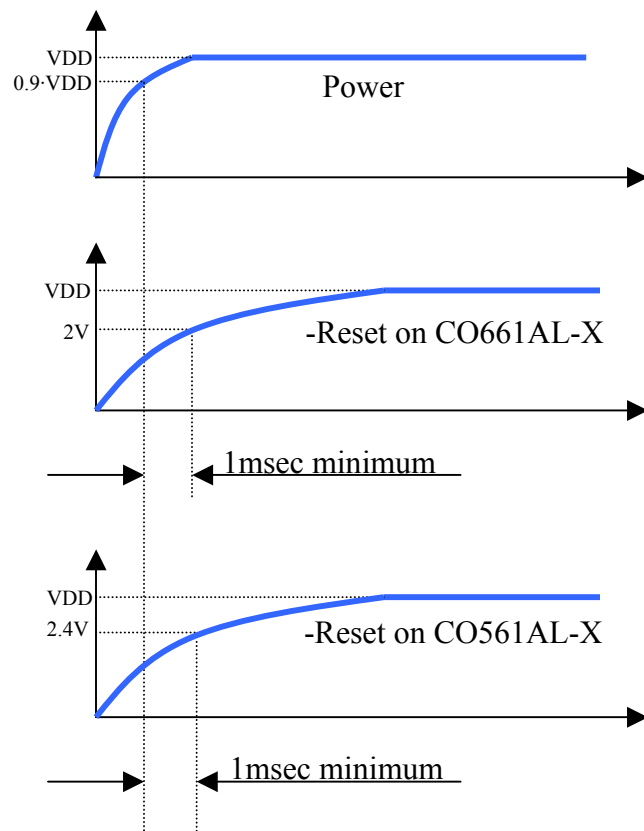


Figure 1: iChip Reset Profiles

Signal Differences

CO661AL-x has a slightly different pin-out definition. The differences respect backwards compatibility with the CO561AD-x family and were introduced in the CO661AL-x family with future extended capabilities in mind. In addition, several signals have additional or new characteristics in the CO661AL-x family. The following table summarizes these differences:

Pin #	CO561AD	Changes	CO661AL
	AD0-AD15	In CO561AD, these pins are time-multiplexed with the address BUS. The ALE signal (pin 41) is used to latch the address. In CO661AL, these pins are pure data BUS. This difference is transparent to the design.	D0-D15
12	-RES	In CO561AD, Vih is 2.4V min. In CO661AL, Vih is 2.0V min. If an RC network is used to reset the iChip, different RC network discrete values may be required.	-RES
14	-UCS	In CO561AD, this pin is used as the internal flash chip-select. In CO661AL, this pin is reserved for future use as a General Purpose I/O (GPIO Z0) and should be left Not Connected (NC).	Z0
15	-DSRH	In CO561AD, this pin has an internal pull down resistor. In CO661AL, this pin must be pulled down to GND externally, if not used.	-DSRH
21	-LCS	In CO561AD, this pin is used for the internal RAM chip-select. In CO661AL serial mode, this pin is reserved for future use as a GPIO (Z1) and should be left NC. In CO661AL parallel mode, this pin is chip select.	Z1/PCS
29	TXDM	In CO661AL, this pin is used to force iChip into tri-state mode for manufacturing purposes. It must be ensured that the TXDM signal is HIGH at least 2 uSec before reset.	TXDM
40	URTINT	In CO561AD, this pin is dedicated for Connect One debugging purposes. In CO661AL serial mode, this pin is reserved for future use as a GPIO (Z2) and should be left NC. In parallel mode, it indicates Output Buffer Empty.	Z2/-POBE

Pin #	CO561AD	Changes	CO661AL
41	ALE	In CO561AD, this pin is used as Address Latch Enable to support the multiplexed Address/Data BUS. In CO661AL, this pin is configurable with an AT+i command. By default, it used to disable the iChip's oscillator (X1 Pin 42) via an external gate in order to achieve full sleep mode with minimal power consumption. It may also be configured as a GPIO (Z3).	PWSG/Z3 ¹
44	CLKO	In CO661AL this signal is configurable. By default it functions as clock out (CLKO), to maintain CO561AD compatibility. In the future, it may be configured to function as a heartbeat (HBT) signal (50% duty cycle, 40 mSec frequency, square wave when iChip F/W is properly running) or as a GPIO (Z6) signal, with the AT+iPN44 command (see AT+i Programmers Manual).	CLKO/HBT/Z6 ²
50	A19	In CO661AL-S, this pin is GPIO (Z7) by default. In CO561AD-x and CO661AL-L or D, it is A19.	A19/Z7
61	HLDA	The CO661AL-x family does not support DMA. In CO661AL, this pin is reserved as GPIO (Z4) and should be left NC.	Z4
62	HOLD	The CO661AL-x family does not support DMA. In CO661AL, this pin is reserved as for future use as a GPIO (Z5) and should be left NC.	Z5
55	GND	In the CO661AL, this pin is serial/parallel select and must be grounded for serial mode. CO561AD compatibility is assured when this pin is at GND. When this pin is pulled up, CO661AL-x devices will boot in parallel host mode. Several pin definitions are different in parallel mode. See CO661AL-x datasheets for additional information.	-SER/PAR
15	-DSRH	In CO661AL parallel mode, this pin is an input signal used to reset the parallel circuit	-DSRH/-PRES
58	-RTSH	In CO661AL parallel mode, this pin is an output signal used to indicate an error in the parallel circuit.	-RTSH/-PERR
59	-CTSH	In CO661AL parallel mode, this pin is an output signal used to indicate that the parallel input buffer is full.	-CTSH/PIBF

Table 1: CO561AD vs. CO661AL Signal Differences

Notes: 1 – AT+i command to configure pin 41 shall be introduced in firmware version 8.01

2 – AT+i command to configure pin 44 shall be introduced in firmware version 7.04